SOLE INVENTOR

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APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, Byoung Hee Cho, a citizen of the Republic of Korea, residing at 433-7 Changjeon-Dong, Ichon-Shi, Kyungki-Do (467-807), Korea, have invented a new and useful METHOD FOR FORMING GATE OXIDE IN SEMICONDUCTOR DEVICE, of which the following is a specification.

METHOD FOR FORMING GATE OXIDE IN SEMICONDUCTOR DEVICE

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a method for forming a gate oxide film of a semiconductor device, and more specifically, a method for forming a gate oxide film of a semiconductor device capable of reducing amounts of electrons and holes, which are trapped in the oxide film.

2. Discussion of Related Art

[0002] An electrically erasable programmable flash memory cell demands a high voltage at the time of programming or erasing operation. Repetition of the programming and erasing operations with the high voltage results in occurrence of traps of electrons and holes in the gate oxide film of the flash memory cell. In turn, the electrons and holes trapped in the gate oxide film shift the gate voltage, which is applied to the gate of the cell. For example, if the programming and erasing operations are repeated by 10,000 to 1,000,000 times, the accumulation of the trapped charges shift the threshold voltage of the cell.

[0003] The trap of charges in the oxide film can be reduced by using a nitride oxide film. Namely, the occurrence of the trap of the charges can be suppressed by forming a barrier layer, which is made by combination of an

oxide and nitrogen in the direction of the silicon substrate by means of N_2O or N_2 treatment at the time of growing the oxide film.

[0004] However, in case of the flash cell, the current flow occurs at both ends of the gate. Therefore, although the trap of charges in the direction of the silicon is suppressed by the barrier formed by the oxide and the nitrogen, the trap of charges in the direction of the polysilicon cannot be suppressed since there is no barrier formed by the oxide and nitrogen. Namely, the trap of charges in the direction of the substrate is suppressed, but the trap of charges in the direction of the polysilicon is not suppressed.

[0005] Now, a conventional method of forming a gate oxide film will be described with reference to Figs 1A to 1C.

[0006] As shown in Fig. 1A, a well formation process and an ion implantation process for controlling a threshold voltage of a cell are carried out on the semiconductor substrate 10. Next, a gate oxide film 20 is formed by using an oxidation process, and then, a polysilicon film 30 is formed above the gate oxide film 20.

[0007] Referring to Fig. 1B, a nitride film 40 is formed above the polysilicon film 30.

[0008] Fig. 1C is a cross-sectional view illustrating a state that the gate oxide 20 and a device isolation film are formed by performing a patterning process, a self-aligned contact oxidation process, an HDP oxide film burying process, and a nitride film removing process for forming a device isolation film.

[0009] As described above, in case of the conventional method, the current flow occurs at both ends of the gate. Therefore, although the trap of charges in the direction of the silicon is suppressed by the barrier formed by the oxide and the nitrogen, the trap of charges in the direction of the polysilicon cannot be suppressed since there is no barrier formed by the oxide and nitrogen. Namely, the trap of charges in the direction of the substrate is suppressed, but the trap of charges in the direction of the polysilicon is not suppressed.

SUMMARY OF THE INVENTION

[0010] The present invention is directed to a method of gate oxide film of a semiconductor device capable of suppressing a trap of charges in a direction of a polysilicon as well as suppressing a trap of charges in a direction of a semiconductor substrate.

[0011] One aspect of the present invention is to provide a method for forming a gate oxide film of a semiconductor device comprising the steps of; forming a gate oxide film and a polysilicon film sequentially on a semiconductor substrate; performing a nitrogen ion implantation process for the semiconductor substrate including the gate oxide film and the polysilicon film; performing a thermal treatment process to form barrier layers by combination of oxides and nitrogen at an interface between the semiconductor substrate and the gate oxide film, and at an interface between the gate oxide film and the polysilicon film; and forming a nitride film on the polysilicon film.

[0012] In the aforementioned of a method for forming a gate oxide film of a semiconductor according to another embodiment of the present invention, the thermal treatment process is performed by an RTP spark annealing process.

[0013] In the aforementioned of a method for forming a gate oxide film of a semiconductor according to another embodiment of the present invention, the nitrogen ion implantation process is performed by using a source gas including N^+ or N_2^+, with a dose of 1E14atoms/㎠ to 1E16atoms/㎠ and an implantation energy of 1keV to 20keV.

[0014] In the aforementioned of a method for forming a gate oxide film of a semiconductor according to another embodiment of the present invention, the RTP spark annealing process is performed at an N_2 gas ambient, a ramp up temperature is about 100℃/sec, and the RTP temperature is 900℃ to 1100℃.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figs. 1A to 1C are cross-sectional views for explaining a method of forming a gate oxide of a semiconductor device in accordance with a conventional method.

[0016] Figs 2A to 2D are cross-sectional views for explaining a method of forming a gate oxide of a semiconductor device in accordance with the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0017] Now the preferred embodiments according to the present invention will be described in detail with reference to the accompanying drawings.

[0018] Figs 2A to 2D are cross-sectional views for explaining a method for forming a gate oxide of a semiconductor device in accordance with the present invention.

[0019] As shown in Fig. 2A, a well formation process and an ion implantation process for controlling a threshold voltage of a cell are carried out on the semiconductor substrate 10. Next, a gate oxide film 20 is formed by using an oxidation process, and then, a polysilicon film 30 is formed above the gate oxide film 20.

[0020] Fig. 2B is a cross-sectional view illustrating a state that a nitrogen ion implantation process is carried out to implant the nitrogen ion at the interface of the polysilicon film 30 and the gate oxide film 20, and then, an rapid thermal processing (RTP) is performed at an N_2 gas ambient. By the thermal treatment process, the nitrogen and the oxide at are reacted at an interface between the semiconductor substrate 10 and the gate oxide film 20, and at the interface between the polysilicon film 30 and the gate oxide film 20 to form barrier layer. By doing so, the trap of charges in the direction of the semiconductor substrate as well as the trap of charges in the direction of the polysilicon is suppressed. The nitrogen ion implantation process is performed by using a source gas including N^+ or N_2^+, with a dose of 1E14atoms/㎠ to 1E16atoms/㎠ and an implantation energy of 1keV to 20keV. The thermal treatment process is carried out by using an RTP spark annealing process. The

RTP spark annealing process is performed at an N_2 gas ambient, a ramp up temperature is about 100℃/sec, and the RTP temperature is 900℃ to 1100℃.

[0021] The barrier layers formed in both directions function as barriers against the traps of the electrons and the holes, which occur in the both directions at the time of the programming and erasing operations on the flash cell, so that it is possible to effectively avoid the shift of the gate voltage applied to the gate of the cell.

[0022] Referring to Fig. 2C, a nitride film 40 is formed above the polysilicon film 30.

[0023] Fig. 4D is a cross-sectional view illustrating a state that the gate oxide 20 and a device isolation film 50 are formed by performing a patterning process, a self-aligned contact oxidation process, an HDP oxide film burying process, and a nitride film 40 removing process for forming a device isolation film.

[0024] As described above, according to the present invention, it is possible to reduce the amount of the trapped charges which occur due to the current flow in the gate oxide at the time of the programming and erasing operations of a NAND flash memory cell by using the barrier layers formed in both directions due to reaction of the oxide and the nitrogen, thereby being capable of suppressing the shift of the threshold voltage.

[0025] The avoidance of the shift of the threshold voltage of the cell by using the barrier layers in both directions results in the preservation of uniform characteristics of the cell at the repetition of the programming and erasing

operations, so that it is possible to improve the characteristics associated with the programming and erasing operations.

[0026] In addition, in case of an NAND flash memory, an oxidation-enhanced diffusion (OED) effect is generated due to a thermal treatment process which is carried out before the patterning process for forming a device isolation film after the boron implantation process for forming a P well and controlling the threshold voltage of the cell. The OED effect can be reduced by performing the RTP spark annealing process as the N_2 thermal treatment process for combining the oxide and the nitrogen in the gate oxide film, so that it is possible to obtain an uniform threshold voltage of the cell.